REMARKS

The Final Office Action dated March 17, 2006, in this Application has been carefully considered. Claims 22-42 are pending. The above requested amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-21 have been previously cancelled. Claims 28 and 38 have been amended in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Claim 38 and its dependent Claims stand rejected under 35 U.S.C. § 101 as allegedly directed to non-statutory subject matter. In particular, the Examiner stated that the recitation, "a computer program product . . . having a medium with a computer program embodied thereon" does not include a "requirement in the claim for storing the program in a computer readable medium" and thus is "not statutory because it is not capable of casing functional change in the computer." Final Action, at Page 2. Applicants respectfully traverse this rejection.

Nevertheless, Claim 38 has been amended to recite, in relevant part, "the computer program product having a *computer-readable* medium with a computer program embodied thereon." (Emphasis added). Applicants respectfully request that the Examiner enter this amendment as it places the Claims in better condition for appeal by eliminating at least one substantive issue. Additionally, Applicants respectfully request that the Examiner withdraw the rejections of Claim 38 and its dependent Claims under 35 U.S.C. § 101.

Claim 28 stands objected to because of an informality. Claim 28 has been amended in this Response to correct the identified informality. Accordingly, Applicants respectfully request that the Examiner enter the amendment of Claim 28 as it places the Claims in better condition for appeal. Additionally, Applicants respectfully request that the Examiner withdraw the objection to Claim 28.

Claims 22-23, 25-26, 29-30, 32-36, 38, and 40-42 stand rejected under 35 U.S.C. §103(a) by U.S. Patent No. 6,425,058 by Arimilli et al. ("Ar'058") in view of U.S. Patent No. 6,430,656 by Arimilli et al. ("Ar'656"). Insofar as they may be applied against the Claims, these rejections are traversed and overcome.

Regarding Claim 22, Ar'058 and Ar'656 were cited as assertedly fully disclosing the following:

(1) "a system for managing cache replacement eligibility"

comprising (2) "a first address register configured to request an address from an L1 cache (*citing* Ar'058, col. 4, lines 1-30, "registers that contains addresses for fetching instructions and fetching and storing operand in L1 caches, Fig 1");

(3) a "range register configured to generate a class identifier in response to a received requested address and to transmit the requested address and class identifier to a replacement management table coupled to the range register; the replacement management table configured to generate L2 tag replacement control indicia in response to a received requested address and class identifier" (*citing* Ar'656, col. 6, lines 57-67 ("the congruence classes information 'class identifier' in address field 16 is used in the directly Fig 2: #20"); col. 6, lines 1-46 ("information in the directory are used to generate group selector and congruence class selector that determine which cache location to be replaced"));

(4) "an L2 address register coupled to the first address register and configured to request an address from an L2 cache; an L2 cache coupled to the L2 address register and the replacement management table and configured to determine whether a requested address is in the L2 cache and further configured to assign replacement eligibility of at least one set of cache lines in the L2 cache in response to received L2 tag replacement control indicia" (*citing* Ar'656, col. 6, lines 1-46, which

allegedly "clearly describes the congruence classes are mapped into certain associate sets of the cache"); and

(5) "in response to a determination that a requested address in not in the L2 cache, the L2 cache further configured to overwrite a cache line within a set of the 1,2 cache ms a function of the replacement eligibility" (*citing* Ar'656, col. 6, lines 24-36, which allegedly "clearly describes the congruence classes are mapped into certain associate sets of the cache, and allowing the replacement of cache entries"). Final Action, at Pages 4-5.

The Examiner admits that Ar'058 "does not describe the claim's detail of address range register." Final Action, at Page 4. To supply this missing element (and a number of other elements), the Examiner offers Ar'656, stating that "It would have been obvious to one of ordinary skill in the art at the time of invention to include the congruency class cache and address indexing techniques as suggested by Ar'656 in Ar'058's system to map address ranges in cache based on the concurrency group information thereby using the cache more effectively for applications running in multiple processors system." Final Action, at Page 4.

The Examiner's proposed combination fails for a number of reasons.

As the Examiner admits, Ar'058 fails to disclose one of the distinguishing characteristics of the present invention, namely, "a range register coupled to [an] L1 cache," "the range register configured to generate a class identifier in response to a received requested address and to transmit the requested address and class identifier to a replacement management table coupled to the range register" and "the replacement management table configured to generate L2 tag replacement control indicia in response to a received requested address and class identifier," as recited by Claim 22.

Instead, Ar'058 takes a fundamentally different approach to cache management. For example, Ar'058 does not suggest, teach, or disclose the replacement management table generating

L2 cache tag replacement control indicia in response to a received class identifier, with the class identifier generated in response to a requested address. The Ar'058 approach instead teaches "information type fields" in an L2 "cache directory" that specify which type(s) of information an associated cache line can store. Ar'058 states, "information type field 78 [of each directory entry] specifies which type(s) of information the associated set can store." Ar'058, col. 5, lines 47-49. Further, "The cache lines stored within information array 64 are recorded in cache directory 62, which contains one directory entry for each set in information array 64." Ar'058, col. 5, lines 23-25.

Accordingly, the information type field of Ar'058's L2 cache determines which information type or types an associated cache set can store. In contrast, in the system as recited in Claim 22, the L2 cache is "configured to assign replacement eligibility of at least one set of cache lines in the L2 cache in response to received L2 tag replacement control indicia." As described above, the L2 tag replacement control indicia are generated "in response to a received requested address and class identifier." Thus, in the system as recited in Claim 22, replacement eligibility of one or more sets of a cache is assigned in response to the tag replacement control indicia, which is itself a function of the requested memory address and the class identifier. Rather than assigning information types that sets can store, as is done in Ar'058, the present invention identifies eligible replacement sets based on an address and class identifier.

Despite these fundamentally different approaches, the Examiner offers Ar'656 to supply elements missing from Ar'058. Given that Ar'058's approach is so different from the claimed approach here, it quickly becomes clear that elements pasted onto Ar'058 from Ar'656 are either inconsistent with Ar'058's approach, teach away from the claimed invention, or otherwise do not show the claimed invention.

First, Ar'656 teaches a cache system that maps a number of "congruence classes" into a "partition", which maps onto several "pages" of memory. *See, e.g.*, Ar'656, col. 5, line 50 to col. 6, line 5. This partitioning serves two express functions. The first function is that the "congruence class partitioning divides the use of the cache with respect to *information type*." Ar'656, col. 2, lines 10-11 (emphasis added). The second function is that "typically a portion of the address field of a memory location is used to partition the distribution of values from memory across the congruence class *sets*." Ar'656, col. 2, lines 11-12 (emphasis added). Thus, in Ar'656, the congruence class is a function of the information type, and the associated set is a function of part of the memory address. In Ar'058, however, "As in conventional set associative caches, memory locations in system memory 20 are mapped to particular *congruence classes* within information array 64 utilizing predetermined index bits within the system memory address." Ar'058, col. 5, lines 9-12 (emphasis added).

Further, Ar'656 introduces an additional restriction: "in order to maintain critical blocks pinned in [the partition], the other blocks in excess of the associativity [sic] number that are mapped to [the partition] *should be unused*." Ar'656, col. 5, line 66 to col. 6, line 1 (emphasis added). These blocks are kept unused, otherwise, "the loading of values from the other blocks may cause the values from the pinned block to be overwritten (victimized and flushed from the cache)." Ar'656, col. 6, lines 1-4. Thus, Ar'656 modifies how physical pages are mapped to real addresses, through manipulation of the effective use of parts of congruency classes. As such, Ar'656 is not concerned with cache replacement control *per se*.

Accordingly, Ar'656 does not show or teach an L2 cache that is "configured to assign replacement eligibility of at least one set of cache lines in the L2 cache in response to received L2 tag replacement control indicia" as recited in Claim 22 and as alleged by the Examiner. *See* Final

Action, at page 4. As described above, the L2 tag replacement control indicia are generated "in response to a received requested address and class identifier." Instead, as described above, in Ar'656, the congruence class is a function of the information type, and the associated set is a function of part of the memory address.

Not surprisingly, there is no mention of "replacement control indicia" whatsoever in Ar'656. As such, Ar'656 cannot be said to disclose a range register configured "to generate a class identifier in response to a received requested address", "to transmit the requested address and class identifier to a replacement management table coupled to the range register", or the replacement management table configured "to generate L2 tag replacement control indicia in response to a received requested address and class identifier" as recited in Claim 22.

Other claimed limitations are likewise absent from Ar'656. For example, the Examiner alleges that the description in Ar'656 of congruence classes mapping to certain associate sets of a cache suffices to teach an L2 cache configured "to assign replacement eligibility of at least one set of cache lines in the L2 cache *in response to* received L2 tag replacement control indicia." Final Action, at Page 5 (emphasis added). Applicants respectfully point out that the cited passage describes neither the L2 cache assigning replacement eligibility nor anything whatsoever regarding L2 tag replacement control indicial. *See* Ar'656, col. 6, lines 1-46.

Accordingly, there is no motivation to supply the particular congruence class configurations of Ar'656 with the system of Ar'058, as the proposed combination completely fails to teach the elements as recited in the Claims. That is, even if there were some purpose to combining Ar'656 with Ar'058, which Applicants do not concede, the combination fails to teach each and every element as Claimed. For at least this reason, the Examiner's proposed combination fails.

Claim 29 also recites similar distinguishing characteristics of the present invention as Claim 22, namely, "setting a class identifier to a predetermined value associated with a predetermined range of addresses if the requested address falls within the predetermined range of addresses," "generating tag replacement control indicia in response to the class identifier," and "setting replacement eligibility of a set in the L2 cache in response to the tag replacement control indicia." For at least the forgoing reasons, the Examiner's proposed combination likewise fails to teach each and every element of Claim 29.

Claims 38 and 41 recite similar limitations as Claims 22 and 29. As such, the Examiner's proposed combination likewise fails to teach each and every element of Claims 38 and 41.

In view of the foregoing, it is apparent that the cited references do not disclose, teach or suggest the unique combinations recited in Claims 22, 29, 38 and 41. Applicants therefore submit that Claims 22, 29, 38 and 41 are clearly and precisely distinguishable over the cited reference in a patentable sense, and are therefore allowable over this reference and the remaining references of record. Accordingly, Applicants respectfully request that Claims 22, 29, 38 and 41 be allowed.

Claims 23-28 depend on and further limit Claim 22. Claims 30-37 depend on and further limit Claim 29. Claims 39-40 depend on and further limit Claim 38. Claim 42 depends on and further limits Claim 41. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that dependent Claims 23-28, 30-37, 29-40, and 41 also be allowed.

Claims 24 and 37 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ar'058 and Ar'656 and further in view of U.S. Patent No. 5,974,507 by Arimilli et al. ("Ar'507"). Applicants respectfully traverse these rejections. In particular, Applicants submit that Claims 24 and 37 are patentable over the Examiner's proposed combination for at least the reasons

that Claims 22 and 29 are patentable. That is, the combination of Ar'058 and Ar'656 fails to teach each and every element of the independent Claims 22 and 29, from which Claims 24 and 37 depend, as described above. For at least this reason, Applicants respectfully request that the rejections against Claims 24 and 37 be withdrawn and that Claims 24 and 37 be allowed.

Claims 27-28, 31 and 39 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ar'058 and Ar'656 and further in view of Ar'507 and U.S. Patent No. 5,708,789 by McClure ("McClure"). Applicants respectfully traverse these rejections. In particular, Applicants submit that Claims 27-28, 31 and 39 are patentable over the Examiner's proposed combination for at least the reasons that Claims 22 and 29 are patentable. That is, the combination of Ar'058 and Ar'656 fails to teach each and every element of the independent Claims 22 and 29, from which Claims 27, 28, and 31 depend, as described above, as well as Claim 38, from which Claim 39 depends. For at least this reason, Applicants respectfully request that the rejections against Claims 27-28, 31 and 39 be withdrawn and that Claims 27-28, 31 and 39 be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 22-42.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

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CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3032
Fax: (214) 760-3003

Theodore F. Shiells
Reg. No. 31,569